18. (New)   A direct memory access controller, said direct memory access controller comprising:

a state logic machine for receiving a single command to provide a range of sequential data words; and

a memory controller for fetching a first portion of the range and a second portion of the range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the single command.

19. (New) The direct memory access controller of claim 18, wherein the memory controller fetches the first portion of the range and the second portion of the range in a forward address order

20. (New) The direct memory access controller of claim 18, further comprising:

a local buffer for storing the first and second portions in a forward address order, said local buffer comprising a plurality of data words.

21. (New) The direct memory access controller of claim 20, wherein the plurality of data words of the local buffer are narrower in width than the sequential data words.

22. (New) The direct memory access controller of claim 20, further comrprising:

a port for transmitting the contents of the plurality of data words of the local buffer in a reverse

address order.

23. (New) The direct memory access controller of claim 22, further comprising:

at least one multiplexer for reversing the bit positions of contents of at least one of the data words of the local buffer.

24. (New) A method for fetching data words, said method comprising:

receiving a single command to provide a range of sequential data words, starting a beginning address and ending at an ending address;

fetching a portion, in a forward address order, of the range of sequential data words, said wherein said portion of the range of sequential data words consists of the predetermined amount of data words that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to a capacity of a local buffer;

fetching, in the forward address order, at least one preceding portion of the range of sequential data words, wherein each of the preceding portions of the range of sequential data words consist of the predetermined amount of data words; and

wherein a one of the preceding portions of the range of sequential data words comprises the beginning address, truncating those data words that precede the beginning address.

25. (New) The method of claim 24, further comprising:
loading the portion and the at least one

preceding portions of the sequential data words into the local buffer.

26. (New) The method of claim 25, further comprising:
reversing the portion and the at least one preceding portions of the range of sequential data words.

27. (New) The method of claim 26. further comprising:
reversing the truncated one of the preceding portions of the range of sequential data words that comprises the beginning address.